AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listing, of claims in the specification:

1. (Currently amended) A circuit coupled to an output device, the circuit comprising at least one transistor device comprising at least one p-channel device, said at least one transistor device adapted to limit a duration of a high voltage across the output device thereby reducing hot carrier injection stress.

2. (Original) The circuit of Claim 1, further comprising two stacked transistor devices coupled to the output device.

3. (Currently amended) The circuit of Claim 1, wherein ~~said transistor device comprises~~ said at least one p-channel transistors coupled to the output device.

4. (Original) The circuit of Claim 1, wherein said transistor device comprises two stacked p-channel transistors coupled to the output device.

5. (Original) The circuit of Claim 1, wherein the output device comprises at least one n-channel output transistor.

6. (Original) The circuit of Claim 1, wherein the output device comprises two stacked n-channel transistors.

7- 8. (Cancelled)

9. (Currently amended) An integrated circuit comprising:

an IO PAD;

an output circuit coupled to at least said IO PAD; and

a stress circuit comprising at least one p-channel transistor, said stress circuit coupled to at least said output circuit and adapted to limit a duration of a high voltage

across said output circuit when said output circuit is enabled, thereby reducing stress on said output circuit.

10-11. (Cancelled)

12. (Currently amended) The integrated circuit of Claim ~~10~~ 9, wherein said at least one p-channel transistor comprises two stacked p-channel transistors.

13. (Original) The integrated circuit of Claim 9, wherein said output circuit comprises at least one transistor.

14. (Original) The integrated circuit of Claim 13, wherein said transistor comprises an n-channel transistor.

15. (Original) The integrated circuit of Claim 13, wherein said transistor comprises two stacked n-channel transistors.

16. (Currently Amended) ~~The~~ A method of controlling hot carrier injection stress comprising limiting a duration of a high voltage across an output device using a stress circuit comprising at least one p-channel transistor to limit said duration of said high voltage across said output device when said output device is enabled.

17. (Cancelled)

18. (Currently amended) A method of reducing stress across an output circuit, comprising:

determining if the output circuit is tri-stated;

determining if a PAD voltage is greater than a predetermined voltage level;

enabling the output circuit;

turning on a stress circuit comprising at least one p-channel transistor, dissipating a voltage across the output circuit; and

preventing the output circuit from experiencing HCI stress.

19-21. (Cancelled)